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System-on-Chip (SoC) Technology for Tokamak Electron Cyclotron Emission Imaging and Microwave Imaging Reflectometry

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The importance of Microwave imaging instruments for diagnosis of electron temperature fluctuations (electron cyclotron emission imaging-ECEI) and electron density fluctuations (microwave imaging reflectometry-MIR) is attested to by their implementation on a number of tokamaks including ASDEX-Upgrade, DIII-D, EAST, J-TEXT, and KSTAR where they have facilitated diverse physics studies including Alfvén eigenmodes, ELM suppression and disruptions, and sawtooth reconnection[1-5]. We may now report on two major technological improvements:

1- By adding a V-Band (50 – 75 GHz) MMIC LNA (gain ~ 15 dB and noise temperature ~ 500 K) before the mixer diode, the overall noise temperature is reduced from as much as 250,000 K to as little as 2,000 K[6].

2- A new system-on-chip (SoC) approach is capable of not only incorporating improvement in system noise temperature, but also provides a) shielding against interference from RF heating and strong bursts of mm-wave radiation that sometimes originate in the plasma, and b) the ability to amplify and multiply low-frequency sources to generate high-frequency LO signals directly on the individual chips.

Improved noise temperature facilitates absolute temperature calibration, which is of vital importance for obtaining electron temperature profiles. Another important benefit pertains to the MIR systems, where pre-amplification significantly lowers the LO power requirement for each channel. This permits an increased number of channels for wider plasma coverage. Shielding against interference provides better data in more challenging experiments. And on-chip LO multiplication eliminates the need for bulky and expensive LO waveguide and LO optics.

First, commercially available GaAs MMICs including the low-noise pre-amplifier, mixer, LO multiplier chain, and IF amplifier were combined on a liquid crystal polymer (LCP) substrate as a proof-of-principle demonstration in the upper V-Band (60-75 GHz)[7].

Next, a compact "system-on-chip" (SoC) approach was undertaken where complete GaAs chip receivers including mm-wave LNA, balanced mixer, x6 LO multiplier chain, and microwave IF amplifier are mounted in waveguide horn antenna enclosures and stacked to form an array within a shielded enclosure[8]. This technology is being installed as a new imaging instrument on DIII-D. For the initial tests, it will take the place of the current low field side ECEI array. Minor modifications of the optics allow the new antennas to preserve the imaging performance.

Upon demonstrating improved noise temperature and shielding, the new instrument will be used to diagnose edge-localized modes and fluctuations of the high-confinement, or H-mode, pedestal. This has never before been achieved for the most ITER-relevant, low-collisionality regimes found on DIII-D, where transient bursts of radiation have limited past investigations.

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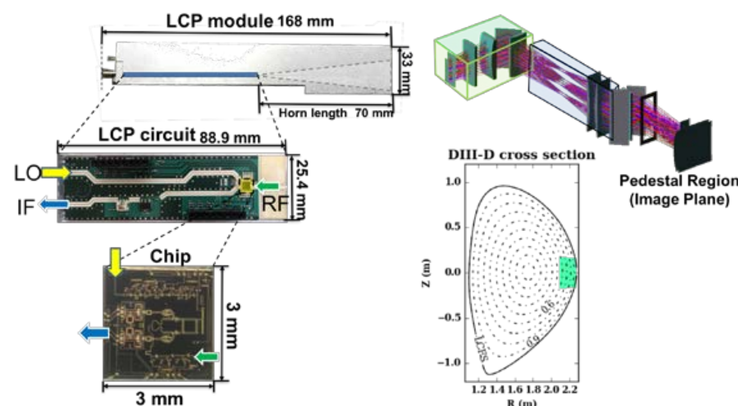

Figure 1 Receiver horn array assembly featuring integrated receiver chips and DIII-D optical arrangement