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# Plasma-induced electronic defects: formation and recovery kinetics in silicon

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In semiconductor devices, electronic defects play important roles in the device performance. The defects can be generated during the device fabrication processes, where plasma processing is used for deposition, etching and surface treatment. The defects are mostly recovered by postannealing; however, some defects remain in the devices, which limits the device performance. So, the suppression of those defects is important for further improvement of the semiconductor devices. Here, we focus on the electronic defects in crystalline silicon (c-Si) created during growth of an hydrogenated amorphous silicon (a-Si:H) passivation layer by plasma-enhanced chemical vapor deposition (PECVD) [1,2].

The generation and annihilation of defects are monitored via in-situ photocurrent measurement in silicon-on-insulator (SOI) during a-Si:H growth by PECVD, as shown in Fig. 1 [1]. An a-Si:H layer is deposited over the SOI in capacitively coupled 60MHz discharge in parallel-plate configuration. The gas pressure is set at 0.3 Torr by regulating a gas flow rate of 50 sccm. The discharge is maintained by supplying a discharge power at 5W. The sample is heated at a temperature of 180 ◦C.

Figure 2(a) shows the time evolution of the photocurrent, $I_p$, in the SOI during growth of a-Si:H and postannealing. The growth of a-Si:H layer is separated into 6 stages. In each growth, the discharge period is set at 10 s, yielding an increment of the layer thickness by 3.0 nm. As shown, $I_p$ is increased with the number of growth, i.e., the layer thickness, except for the first growth of an ultra-thin layer of a-Si:H. The increase in $I_p$ means the termination of defects on the SOI surface, i.e., the surface passivation. This increase exhibits a tendency to be saturated for a thick layer. Such a saturation tendency suggests that the surface passivation requires a certain thickness of an a-Si:H layer, e.g., ~10nm at the present condition.

The effect of H atoms on the generation of defects in the SOI is examined by the experiment where the SOI is treated with $H_2$ plasmas [3]. Figure 2(b) shows the time evolution of Ip in the SOI during $H_2$ plasma treatments and postannealing. The treatment time is varied from 1 ms to 100 s. As shown, each treatment causes a reduction in $I_p$, indicating the generation of defects in the SOI. The reduction is enhanced for a long-time treatment. For instance, $I_p$ is reduced by one order of magnitude for a treatment at 100 s, compared with that before any treatments. For such a large amount of defect generation, the SOI surface is disordered (see Fig. 3). [3].

The defect generation and annihilation in an a-Si:H layer are also studied. Figure 2(c) shows the time evolution of $I_p$ in a sole a-Si:H layer over a glass substrate. As apparent, $I_p$ is significantly increased with the number of growth. Comparing the levels of $I_p$ between 3.0 nm and 18.0 nm-thick layers, $I_p$ is smaller for the 3.0 nm-thick layer by more than two order of magnitude. This highly suppressed $I_p$ for the 3.0 nm-thick ultrathin layer reveals that an ultrathin layer contains a large amount of defects. So, c-Si surface is not passivated with such an ultrathin layer of a-Si:H.

During postannealing, the defects in the SOI and the a-Si:H layer are annihilated. The annihilation is clearly indicated by the increase in $I_p$ for a sole SOI (Fig. 2(b)). and also for a sole a-Si:H layer (Fig. 2(c)). On the other hand, $I_p$ in the SOI of the a-Si:H/SOI stack structure shows different behavior (Fig. 2(a)); $I_p$ is rapidly increased immediately after the growth, and then decreased gradually, approaching to a saturation value. The rapid increase is observed similarly to those two cases of the sole SOI and the sole a-Si:H. However, the decreasing behavior of $I_p$ during postannealing is observed only for the a-Si:H/SOI stack. It suggests that the defects are created at the interface between the a-Si:H layer and the SOI; the interface defects are formed in the a-Si:H/SOI stack by postannealing.

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[1] S. Nunomura et al., Appl. Phys. Express 12, 051006 (2019).
[2] S. Nunomura et al., Phys. Rev. Appl. 10, 054006 (2018).
[3] S. Nunomura et al., AIP Advances 9, 045110 (2019).

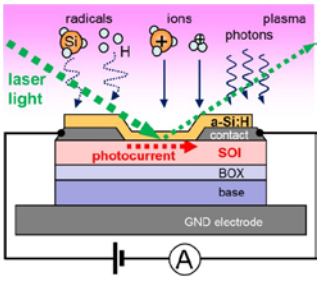


Fig. 1. Experimental setup.

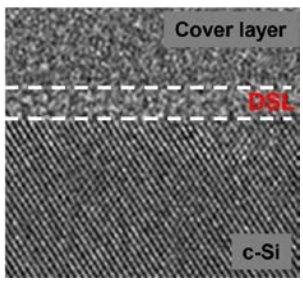


Fig. 3. TEM image.

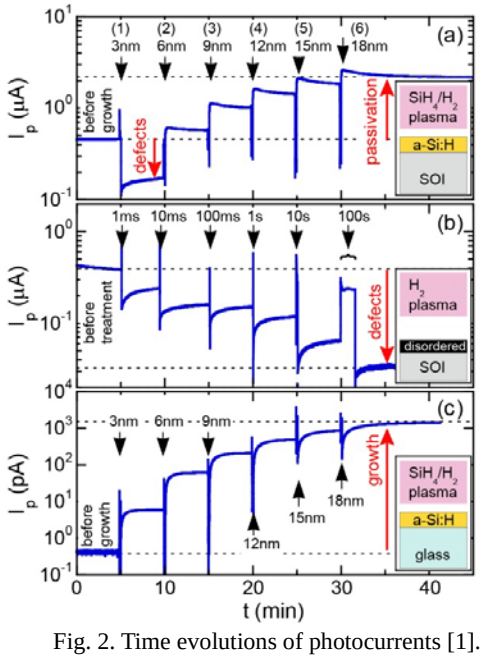


Fig. 2. Time evolutions of photocurrents [1].